BEOL NEM Relay-Based Inductorless DC-DC Converters

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***Abstract*—In the past few years, Back-End-of-Line (BEOL) Nano-electromechanical (NEM) relays have emerged as promising switching devices for the beyond-CMOS era, due to their zero-leakage current property, and the compatibility to CMOS fabrication processes. Though the mechanical movement causes the relays to be inherently slower than transistors, the metallic contact interface untethers the limitation on gate-to-drain voltage, which makes the relays capable of handling higher voltages. In this work, we propose novel designs for BEOL NEM relay-based inductorless DC-DC converters for on-chip voltage conversions. The design, implementation, and analysis of buck (step-down) and boost (step-up) converters are shown. Both converters consist of only four NEM relays, respectively. By utilizing the charge pump topology in a switched-capacitor configuration, the relay converters exhibit lower output ripple and higher efficiency compared to their CMOS counterparts. This is particularly valuable for DC-DC voltage conversions in the Internet of Things chips, where the converter switching frequency is moderate, while the demands for efficiency, area saving, and on-chip integration are high.**

Keywords—Back-end-of-line, nanoelectromechanical relay, buck converter, boost converter, charge pump, switched capacitor.

I. Introduction

Due to the abrupt switching behavior and the zero-leakage property [1, 2], the electromechanical relay has gained increasing research interests on very large scale integration (VLSI) applications. Since then, various explorations on relay structures, materials, and operating environment have been demonstrated on electromechanical relay-based low power computing [3-6]. Toward all relay circuits and systems, efforts have been made on logic functions [7], arithmetic circuits [8], field-programmable gate arrays (FPGAs) [9], and energy management applications [10].

The development of air gap technology in the BEOL process [11] enabled the BEOL relay designs [12]. This makes the relay fully compatible with CMOS (complementary metal-oxide-semiconductor) fabrication processes and metal layers. In addition, by constructing the relay vertically, it dramatically reduces the device footprint, which is another crucial factor in integrated circuits. As a result, unique pass-relay logic and its circuit applications were studied in [13], relay data converter circuits for input/output interface were proposed in [14], and relay memory cell arrays were reported in [15].

The requirement of operating voltage level differs across each part of the chip, and the design of on-chip power converters with relays has not been extensively investigated. Although a preliminary exploration was reported in [16], a large number of relays used makes the design rather infeasible. In this work, we design both the buck converter and the boost converter with only four BEOL NEM relays in an inductorless configuration, for on-chip voltage regulations. Unlike CMOS transistors which face a constraint on maximum gate-to-drain voltage due to the oxide breakdown concerns, the metallic contact of relays gives them the capability of handling higher voltages.

II. Relay Structure and its Operation

A. Relay Structure

The BEOL NEM relay, shown in Figure 1, consists of four terminals: Gate (G), Source (S), Drain (D), and Body (B). The source, drain, and body electrodes are fixed, and the free moving serpentine beam is anchored at the bottom. An inter-metal dielectric (IMD) separates the gate and channel. The inset shows the symbol for the four-terminal relay.

B. Relay Operation

The relay is actuated by the electrostatic force between the gate and the body, as described below:

$$F_e(y, V_{GB}) = \frac{\varepsilon_0 \cdot A_{OV} \cdot V_{GB}^2}{2(g_o - y)^2} \quad (1)$$

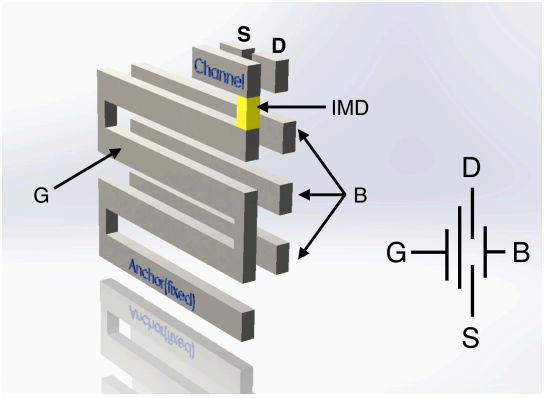


Figure 1: BEOL NEM relay device 3-D structure, electrode arrangements, and its symbol.

where ε_0 is the air permittivity constant, A_{OV} and V_{GB} are the overlap area and the voltage difference between the gate and the body respectively, g_o is the initial gap between the channel and the source/drain electrode, and y is the displacement of the beam, which is constrained in the y-axis only.

If the voltage difference between the gate and the body terminal exceeds the inherent threshold value, known as the pull-in voltage (V_{PI}), the electrostatic force exceeds the spring restoring force, and the channel eventually connects the source and drain, as shown in Figure 2(a). Other technological specifications can be found in Figure 2(b).

The abrupt switching behavior of the relay is observed and plotted in Figure 2(c). The serpentine shaped beam effectively lowers the spring constant of the beam, thus, reduces the actuating voltage needed to turn on the switch to around 2 V. Upon pull-in, the distance between the gate and the body abruptly decreases, results in a sudden increase on the electrostatic force. Together with the Van der Waals force on the metallic contact surface, the relay exhibits a hysteresis between the pull-in voltage and the pull-out voltage (V_{PO}).

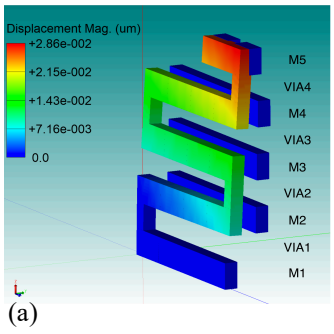
C. Relay Inverter

Since the electrostatic force, caused by the voltage difference between the gate and the body, determines the pull-in behavior exclusively, one can utilize this unique property and configure the same device to be either P-type (closed with low gate voltage) or N-type (open with low gate voltage).

As an example, an inverter circuit built with one P-type relay and one N-type relay is shown in Figure 3(a). We use the relay inverter to measure the mechanical delay. From Figure 3(b), after the input signal goes high (low), it takes about 13 ns for the output to get discharged (charged). This delay is mainly contributed to the mechanical delay of the relay.

III. Relay-Based DC-DC Buck Converter

The proposed relay-based Switched-Capacitor Buck Converter (SCBC) is illustrated in Figure 4. It utilizes a flying capacitor to lower the voltage of the output compared to the input. The SCBC is used in on-chip power management systems due to its inductorless scheme, since inductors cover a large area



Technological Specifications	Value
Total Metal Layers	5
Total VIA Layers	4
Metal and VIA Height (2F)	44nm
Metal and VIA Width (F)	22nm
Metal Length	300nm

(b)

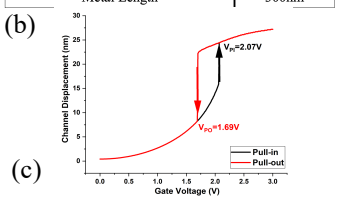


Figure 2: (a) The pulled-in relay: the channel connects the source and drain. The BEOL metal and VIA layers used are indicated next to the structure. The legend indicates the displacement of beam tip on M5 layer. (b) Design specifications of the BEOL NEM relay. (c) DC sweep of the gate voltage for pull-in and pull-out analyses.

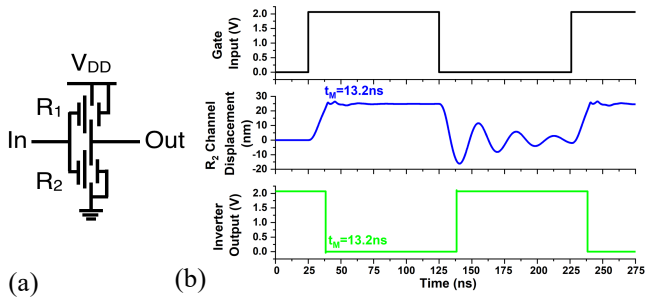


Figure 3: (a) The relay inverter schematic, with R_1 and R_2 relays being configured as P-type and N-type respecrively. (b) Transient response of the relay inverter. When the channel displacement of R_2 relay reaches the initial gap g_0, the discharge path of the inverter output is enabled.

of the chip. Therefore, it desirable to eliminate inductors to have compact power management systems.

A. Operation of the Converter

The converter operates in the following two stages, as illustrated in Figure 5. The blue arrow indicates the current flow during each stage.

- Stage 1: R_1 and R_4 relays are switched on to allow C_{fly} and C to charge in series to achieve 50% of the input voltage.
- Stage 2: R_2 and R_3 relays are switched on to connect C_{fly} and C in parallel and discharge them in the output load.

B. Simulation Setup

Using our custom Verilog-A model, which is validated against a commercial FEM tool, MEMS+ [17], we simulated the relay power converters in Cadence Virtuoso. The operation of the relay buck converter can be seen in Figure 6, with the following specifications: V_{in} = 2.4 V, f_S = 5 MHz, C_{fly} = 100 pF, C = 25 nF, and R = 10 KΩ. The duty cycle is adjusted to be 50%. The output voltage can be expressed as below:

$$V_{out} = \frac{V_{in}}{2 + (4 \cdot \frac{R_{ON}}{R})} \qquad (2)$$

where R_{on} is the contact resistance of the relay when it is pulled-in.

C. Result and Analysis

From the simulation results, the output has a ripple of 0.004%, and the proposed converter has an efficiency of 82.4%.

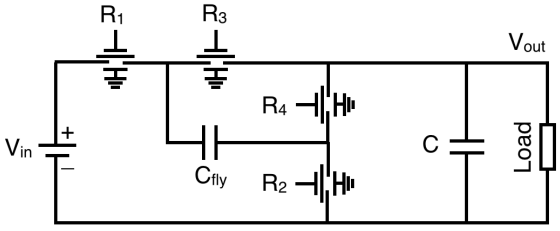


Figure 4: Schematic of relay-based inductorless DC-DC buck converter. C_{fly} is the flying capacitor and C is the output capacitor.

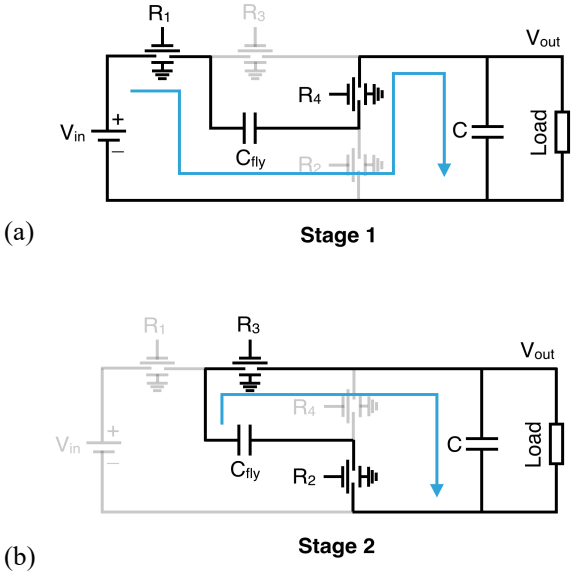


Figure 5: Different operating stages of the relay buck converter. (a) Stage 1, R_1 and R_4 relays are on, both C_{fly} and C are being charged. (b) Stage 2, R_2 and R_3 relays are on, C_{fly} is being discharged.

The implementation of a flying capacitor (C_{fly}) as the charge pump effectively reduces the output ripple. The relay converter efficiency is 17% higher than its CMOS counterpart [18] in 65 nm technology under the same input and output voltage levels and power density [19].

The power loss is mainly due to the relatively high contact resistance of the relay and the 3 ns deadtime (clock overlapping) introduced during the transition of gate inputs. The loss can be further reduced by fine-tuning of the relay operation and its associated passive component values. Though with the inductorless configuration, the proposed converter has a fixed step-down ratio, the conversion scheme based on charge pump gives advantages of area saving, circuit simplicity, as well as a low ripple at the output.

IV. Relay-Based DC-DC Boost Converter

By elaborating on the concept of Switched-Capacitor Voltage Doubler (SCVD) introduced in [20], we implement the boost converter with only four BEOL NEM relays, as described in Figure 7. Similar to the relay buck converter, the inductorless

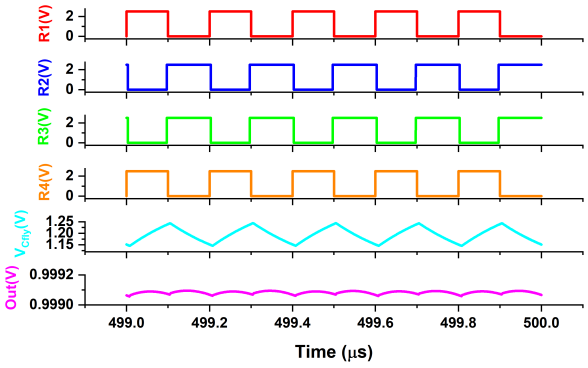


Figure 6: Simulation results of the relay buck converter.

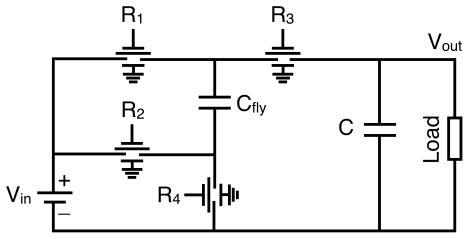


Figure 7: Schematic of relay-based inductorless DC-DC boost converter. C_{fly} is the pumping capacitor and C is the output capacitor.

relay voltage multiplier employs the charge pump capacitor mechanism as well.

A. Operation of the Converter

The converter operates in the following two stages, as depicted in Figure 8. The blue arrow indicates the current flow during each stage.

- Stage 1: R_1 and R_4 relays are switched on, which charges the pump capacitor (C_{fly}) to the input voltage (V_{in}) in the first half cycle of the switching period. The output capacitor C discharges in the output load.
- Stage 2: R_2 and R_3 relays are switched on. The pump capacitor (C_{fly}) is connected in series with the input voltage (V_{in}), which doubles the output voltage compared to the input.

B. Simulation Setup, Resul and Analysis

The below parameters are used for the relay boost converter: V_{in} = 1.2 V, f_S = 5 MHz, C_{fly} = 1 nF, C = 100 nF, and R = 100 KΩ. The duty cycle is adjusted to be 50%. The output impedance of the relay converter is designed to be around 1 Ω,

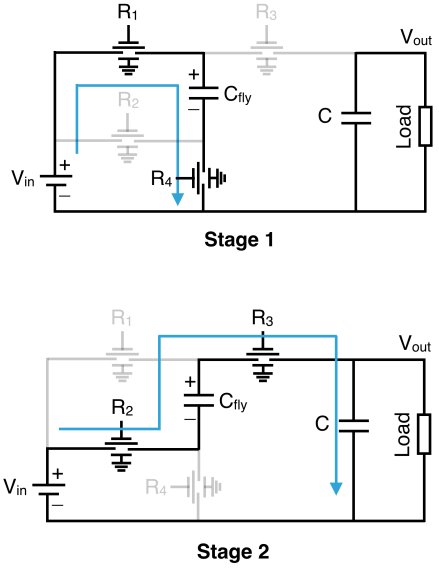


Figure 8: Different operating stages of the relay boost converter. (a) Stage 1, R_1 and R_4 relays are on. C_{fly} is being charged while the output is disconnected from the input. (b) Stage 2, R_2 and R_3 relays are on. C_{fly} is in series with V_{in}, charging the output capacitor.

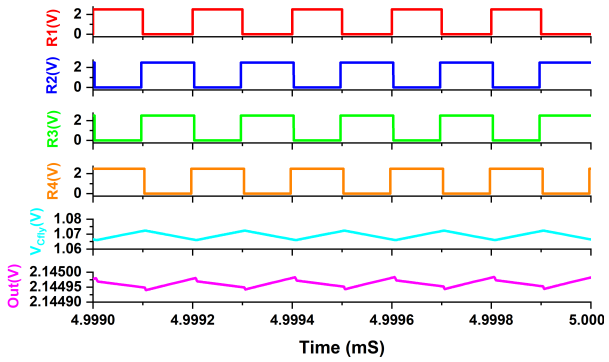


Figure 9: Simulation results of the relay boost converter.

such that it is capable of acting as an ideal voltage source for other parts of the chip. From the simulation results shown in Figure 9, the output voltage ripple is only 0.005%, and the conversion efficiency is 91%. The relay converter has a 14% higher efficiency compared to its CMOS counterpart under the same input and output voltages levels [21]. It also exhibits much smaller output voltage ripple. The losses are mainly coming from the switching and the conduction. Due to the larger output capacitor compared to the relay buck converter, the output of the relay boost converter takes a longer time to settle and reach the final value.

V. Conclusion

This work proposes BEOL NEM relay-based DC-DC buck converter and boost converter for on-chip voltage regulations. By designing the converters with charge pump capacitors, we eliminate the need for the bulky on-chip inductor. The proposed converters are constructed with only four NEM relays respectively, and they present low output voltage ripple, as well as high conversion efficiency. The mechanical delay of the relay limits the maximum operating frequency; however, unlike digital computation which requires high frequency, NEM relays can perfectly cope with the requirement of DC-DC conversions. Moreover, since the voltage conversions are implemented on-chip with high efficiency, they make the relay converters valuable for the development of the Internet of Things.

References

[1] R. Nathanae, V. Pott, H. Kam, J. Jeon, and T.-J. K. Liu, "4-Terminal relay technology for complementary logic," Technical Digest - International Electron Devices Meeting, IEDM, pp. 223-226, 2009. http://dx.doi.org/10.1109/IEDM.2009.5424383

[2] H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon, and T.-J. K. Liu, "Design and reliability of a micro-relay technology for zero-standby-power digital logic applications," in 2009 IEEE International Electron Devices Meeting (IEDM), 2009, pp. 1-4. http://dx.doi.org/10.1109/IEDM.2009.5424218

[3] J. Lee et al., "3-terminal nanoelectromechanical switching device in insulating liquid media for low voltage operation and reliability improvement," in 2009 IEEE International Electron Devices Meeting (IEDM), 2009, pp. 1-4. http://dx.doi.org/10.1109/IEDM.2009.5424380

[4] J. Jeon, V. Pott, H. Kam, R. Nathanael, E. Alon, and T.-J. K. Liu, "Seesaw relay logic and memory circuits," Journal of Microelectromechanical Systems, vol. 19, no. 4, pp. 1012-1014, 2010. http://dx.doi.org/10.1109/JMEMS.2010.2049826

[5] S. Chong et al., "Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage," in 2009 IEEE/ACM International Conference on Computer-Aided Design - Digest of Technical Papers, 2009, pp. 478-484

[6] C. L. Ayala et al., "A 6.7 MHz nanoelectromechanical ring oscillator using curved cantilever switches coated with amorphous carbon," in 2014 44th European Solid State Device Research Conference (ESSDERC), 2014, pp. 66-69. http://dx.doi.org/10.1109/ESSDERC.2014.6948759

[7] M. Spencer et al., "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," IEEE Journal of Solid-State Circuits, vol. 46, no. 1, pp. 308-320, 2011. http://dx.doi.org/10.1109/JSSC.2010.2074370

[8] H. Fariborzi, F. Chen, V. Stojanović, R. Nathanael, J. Jeon, and T.-J. K. Liu, "Design and demonstration of micro-electro-mechanical relay multipliers," in IEEE Asian Solid-State Circuits Conference 2011, 2011, pp. 117-120. http://dx.doi.org/10.1109/ASSCC.2011.6123618

[9] C. Chen et al., "Nano-Electro-Mechanical Relays for FPGA Routing: Experimental Demonstration and a Design Technique," DATE, Proceedings of the Conference on Design, Automation and Test in Europe, pp. 1361-1366, 2012. http://dx.doi.org/10.1109/DATE.2012.6176703

[10] H. Fariborzi et al., "Analysis and demonstration of MEM-relay power gating," in IEEE Custom Integrated Circuits Conference 2010, 2010, pp. 1-4. http://dx.doi.org/10.1109/CICC.2010.5617380

[11] S. Natarajan et al., "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 um2 SRAM cell size," in 2014 IEEE International Electron Devices Meeting, 2014, pp. 3.7.1-3.7.3. http://dx.doi.org/10.1109/IEDM.2014.7046976

[12] N. Xu et al., "Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications," Technical Digest - International Electron Devices Meeting, IEDM, vol. 2015-Febru, no. February, pp. 28.8.1-28.8.4, 2015. http://dx.doi.org/10.1109/IEDM.2014.7047130

[13] R. Li, R. Alhadrami, and H. Fariborzi, "BEOL NEM Relay Based Sequential Logic Circuits," in 2019 IEEE International Symposium on Circuits and Systems (ISCAS), 2019, pp. 1-4. http://dx.doi.org/10.1109/ISCAS.2019.8702123

[14] R. Li and H. Fariborzi, "Ultra-Low Power Data Converters with BEOL NEM Relays," in IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, Canada, 2018. http://dx.doi.org/10.1109/MWSCAS.2018.8623997

[15] K. Kato, V. Stojanović, and T.-J. K. Liu, "Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching," IEEE Electron Device Letters, vol. 37, no. 1, pp. 31-34, 2016. http://dx.doi.org/10.1109/LED.2015.2504955

[16] S. K. Manohar, R. Venkatasubramanian, and P. T. Balsara, "Heterogeneous NEMS-CMOS DCM Buck Regulator for Improved Area and Enhanced Power Efficiency," IEEE Transactions on Nanotechnology, vol. 14, no. 1, pp. 140-151, 2015. http://dx.doi.org/10.1109/tnano.2014.2371992

[17] MEMS+ 6.401 Reference, Coventor MEMS+. [Online]. Available: https://www.coventor.com/mems-solutions/products/mems-plus-overview/.

[18] S. Bang et al., "A fully-integrated 40-phase flying-capacitance-dithered switched-capacitor voltage regulator with 6mV output ripple," in 2015 Symposium on VLSI Circuits (VLSI Circuits), 2015, pp. C336-C337. http://dx.doi.org/10.1109/VLSIC.2015.7231313

[19] M. Steyaert et al. DCDC performance Survey [Online] Available: http://homes.esat.kuleuven.be/~steyaert/DCDC_Survey/DCDC_PS.html

[20] D. Ma and R. Bondade, Reconfigurable switched-capacitor power converters: principles and designs for self-powered microsystems, 1 ed. New York: Springer-Verlag New York, 2013, p. 178.

[21] T. V. Breussegem and M. Steyaert, "A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler," in 2009 Symposium on VLSI Circuits, 2009, pp. 198-199