Assignment 1: Two Stage Amplifier Design using g_m/I_D

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Theory

Being one of the most fundamental blocks in any analog system, Operational Transconductance Amplifiers (OTA) serve many purposes [1]. At its core, it converts input voltage to an output current. While there are a wide variety of topologies, this report focuses on the two stage amplifier implementation (Fig. 1).

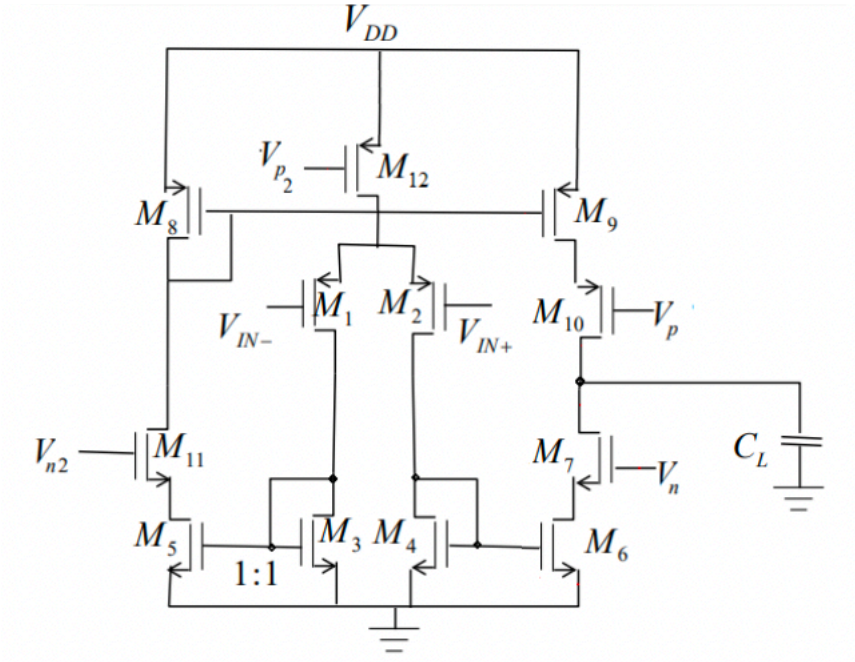

FIGURE 1. TWO STAGE AMPLIFIER.

Following the original paper [2], we will start by understanding the equations relevant to the target specs, namely the DC gain (A_0) and slew rate (SR):

$$A_0 = \left(\frac{g_m}{I_D}\right)_1 * \left(\frac{g_m}{I_D}\right)_2 * \frac{1}{1/(V_{A6} * V_{A7}) + 1/(V_{A9} * V_{A10})}$$

$$SR = \frac{B * I_{D1}}{C_L}$$

where gm/ID_1 is for the input pair, gm/ID_2 is for the cascode transistors at the output stage, B is the current mirror gain ratio, and I_{D1} is the current through the input pairs.

From the equations it is clear that one needs to maximize gm/ID_1 and gm/ID_2 to get the highest gain. At the same time, it is desirable to have sufficiently large B and I_{D1} to meet the SR requirements (>10 MV/s). While trying to adjust for these two metrics, it is also important to keep in mind the phase margin (PM) to ensure stable operation. Lastly, we derive another formulation of the small-signal gain and bandwidth (BW) equations that would prove to be useful later in the design space exploration stage:

$$R_{out} = R_{down} || R_{up} \quad assume \quad R_{down} = R_{up} \rightarrow R_{out} = \frac{R_{down}}{2}$$

$$V_X - I_X * r_{o7} = (I_X - g_{m6,7} V_{GS}) * r_{o7} = (I_X + g_{m6,7} I_X r_{o6}) * r_{o7}$$

$$R_{down} = \frac{V_X}{I_X} = g_{m6,7} r_{o7} r_{o6} + r_{o7} + r_{o6}$$

$$A_0 = g_{m1,2} R_{out} = \frac{1}{2} g_{m1,2} * (g_{m6,7} r_{o7} r_{o6} + r_{o7} + r_{o6})$$

$$BW = \frac{1}{2\pi R_{out} C_L} = \frac{1}{\pi * (g_{m6,7} r_{o7} r_{o6} + r_{o7} + r_{o6}) * C_L}$$

The BW expression was derived assuming that the dominant pole is at the output governed by C_L. These expressions are key because they show us the inverse squared relation ($r_o \propto 1/I_D$) between the gain and the output stage current, which is set by B - the SR parameter. Furthermore, it exposes the direct tradeoff between the DC gain and BW and our knob is I_D of the output stage.

Transistor characterization

The next step is to choose the desired transistor type (SVT, LVT, HVT) from the PDK (we use **GPDK45**) and generate gm/ID plots. Due to their lower V_{TH} we decided to proceed with LVT devices. The setup and the resulting graphs are depicted on Fig. 2-4. We fixed the width of the transistors to 1 um and swept the length from 45 nm to 180 nm. The VDS across transistor was kept at VDD/2 following the convention.

OTA design procedure

Now that we have the look-up plots, we can proceed onto the design stage. In order to maximize both gain and bandwidth, which is our target here, one has to burn a lot of power. In this way, we chose to have I_{D1} = 11 uA and B = 6 so as to stay within the provided current supply limits (100 uA). Then we can figure out the SR:

$$SR = \frac{11e^{-6} * 6}{2e^{-12}} = 33\ MV/s$$

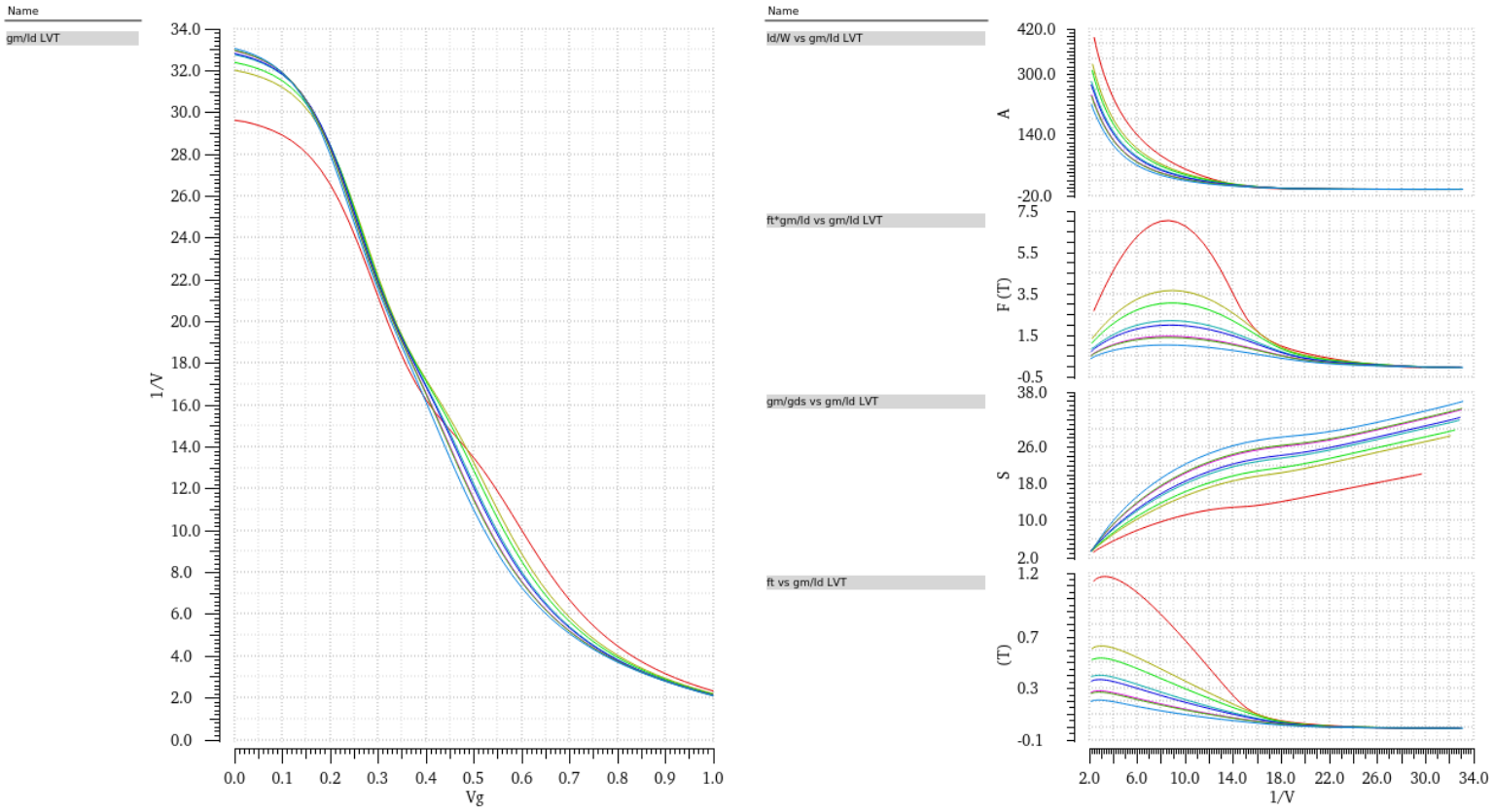

FIGURE 2. GM/ID PLOT FOR NMOS LVT.

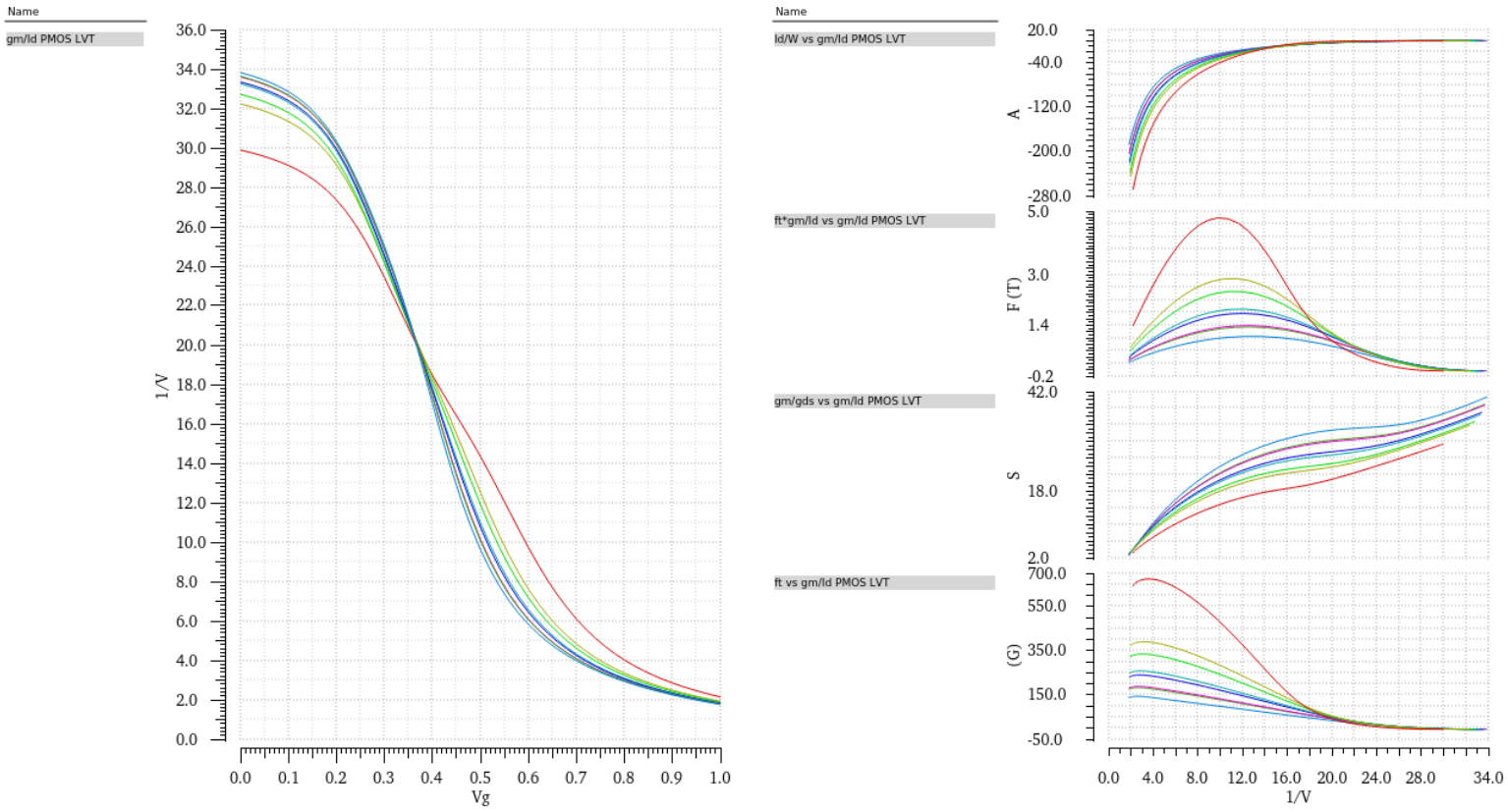

FIGURE 3. GM/ID PLOT FOR PMOS LVT.

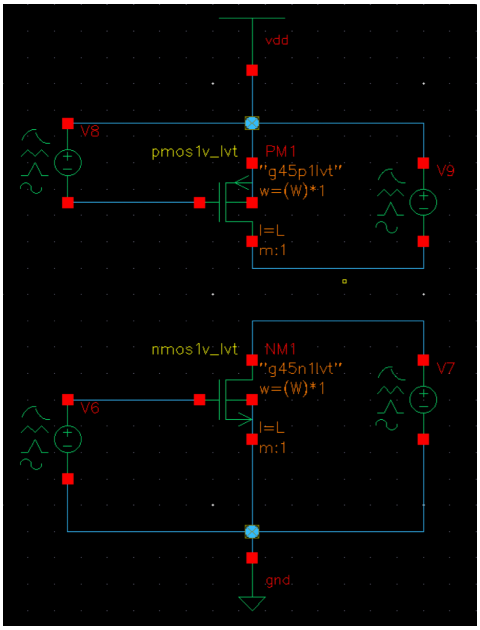

FIGURE 4. TRANSISTOR CHARACTERIZATION SETUP IN CADENCE.

Transistor	W/L theoretical (nm/nm)	W/L adjusted (nm/nm)
M1,2	3972/180	4080/180
M3,4,5	621/180	600/180
M6	3726/180	4200/180
M7	9897/90	9960/90
M8	621/180	580/180
M9	3726/180	4060/180
M10	7765/90	7800/90
M11	1650/90	1560/90
M12	1165/180	2160/180

TABLE 1. DEVICE SIZING.

Now we pick our gm/ID for the input pair. To maximize it, we decided to keep the length of the input pair as well as the current mirror transistors **L = 180 nm**, since this allows much lower threshold voltage and hence higher gm/ID. Thus, based on the V_{TH} of transistor we select the highest gm/ID that still allows us to be above the threshold voltage. In other words, we operate the input pair in the weak-moderate inversion. V_{TH}

for 180 nm transistors is around 330-350 mV and according to Fig. 3-4 (left-side images), if we operate just above it we can get **gm/ID of 21 S** for the input pair. Because we know the current thought the differential pair, we can easily compute the widths of the transistors using the current density plot:

$$W_{1,2} = \frac{I_{D1}}{I_D/W} = \frac{11e^{-6}}{2.76944} = 3972\ nm$$

Next, we turn our attention to the current source transistors. We group them together to have the same gm/ID. The PMOS current source M12 should provide 22 uA current while having high output impedance. For this reason, it's best to operate it in the strong inversion. We set **gm/ID = 11 S** (strong inversion) for all current source transistors and find their W based on their drain current. Following the same math as before, we tabulate all the sizes in Table 1. We also put the sizes for the cascode devices (M7,10,11). The cascode devices' L = 90 nm to lower the threshold voltage and access higher gm/ID in weak-moderate region to maximize the gain. Using the same principle as before (i.e. selecting highest gm/ID that is still above V_{TH}), we set **gm/ID = 16 S** for the cascode devices. After sizing all the devices, we made further adjustment to fine-tune the current values in each branch and make sure every transistor operates in saturation. As can be concluded from Table 1, the final sizes for all devices agree very

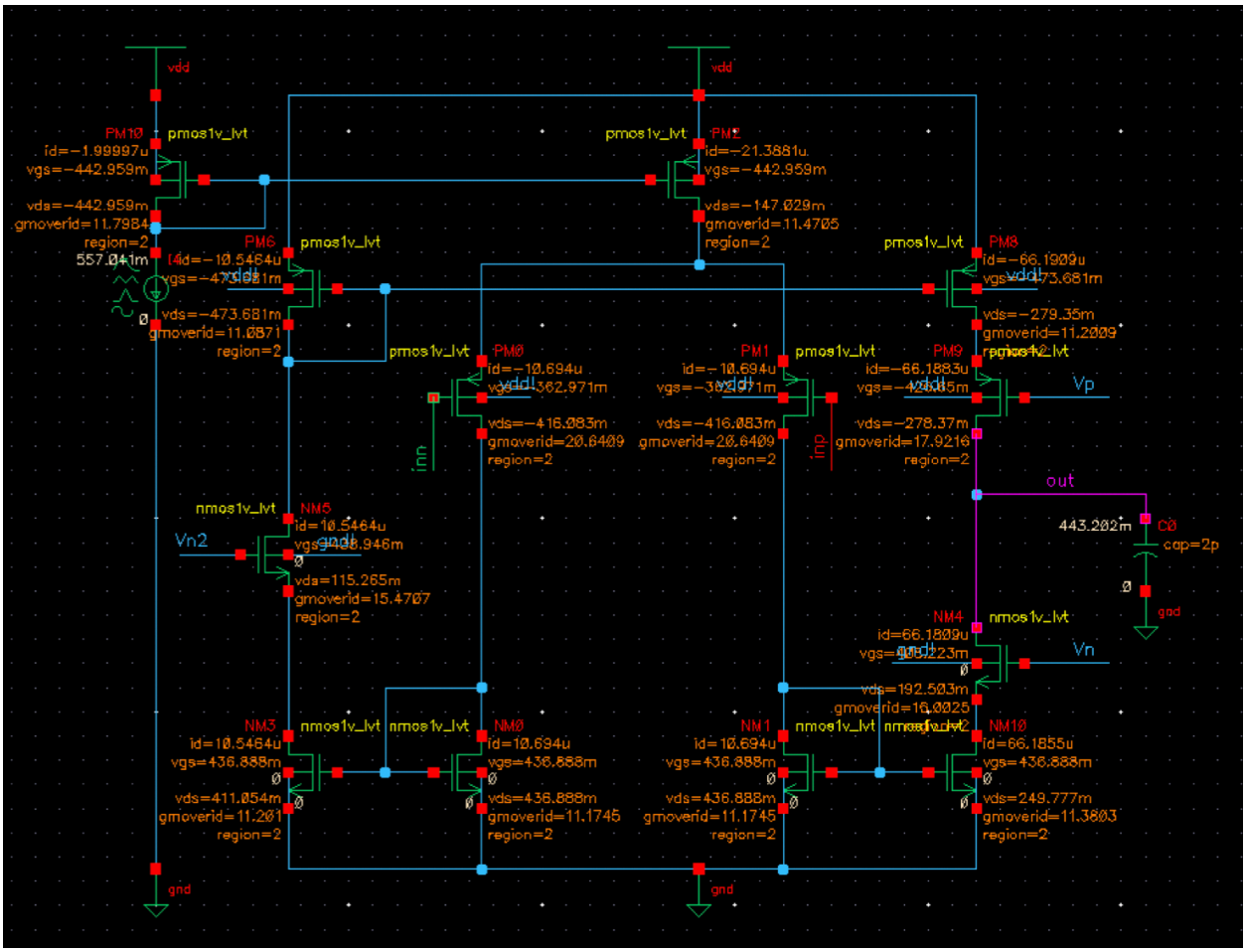

FIGURE 5. CADENCE SCHEMATIC OF THE OTA.

well with the pre-computed ones, all but M6,9, and M12. For M12 we had to increase the size significantly because it was consuming too much V_{DS}. In the case of M6,9 we had to set B to 7 instead of 6 to achieve 66 uA current on the output stage. The final tweaks has to be made to the biasing voltages of M7,10,11 as well as the input pair. For the latter, we decided to have $\mathbf{V_{in,bias} = 490\ mV}$ to achieve the set gm/ID while preserving the current sources in saturation. M11 was biased based on its drain and source voltages so as to keep it in saturation while maximizing the V_G ($\mathbf{V_{n2} = 850\ mV}$). For M7 and M10:

$$M10 : V_G - V_S \leq V_{TH} \quad \rightarrow \quad V_G \leq 719mV - 425mV = 294mV$$

$$M7 : V_G - V_S \geq V_{TH} \quad \rightarrow \quad V_G \geq 252mV + 406mV = 658mV$$

We plug-in these numbers for the V_n and V_p. If one tries to increase V_n and decrease V_p further, this will cause reduction in the output swing coming from the saturation condition equations. Note that we obtain the V_S and V_{TH} values from simulations.

Results

The results of simulation are shown in Fig. 6-9. The performance of the circuit is numerically provided in Table 2. Thus, as can be seen from the results, we successfully met all the specifications and achieved very high gain as well as high BW, though at the cost of maximum power consumption and area. Overall, this report proved that it is possible to achieve one's target specifications within merely a few iterations using the gm/ID methodology.

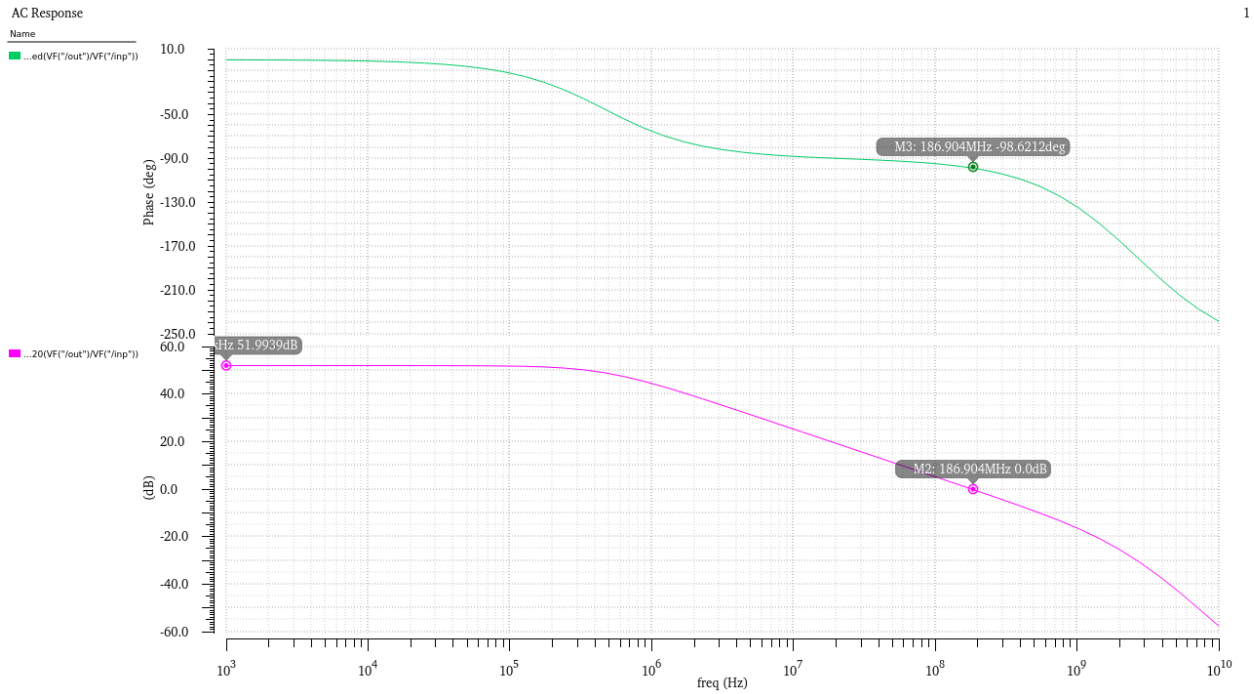

FIGURE 6. GAIN AND PHASE PLOTS.

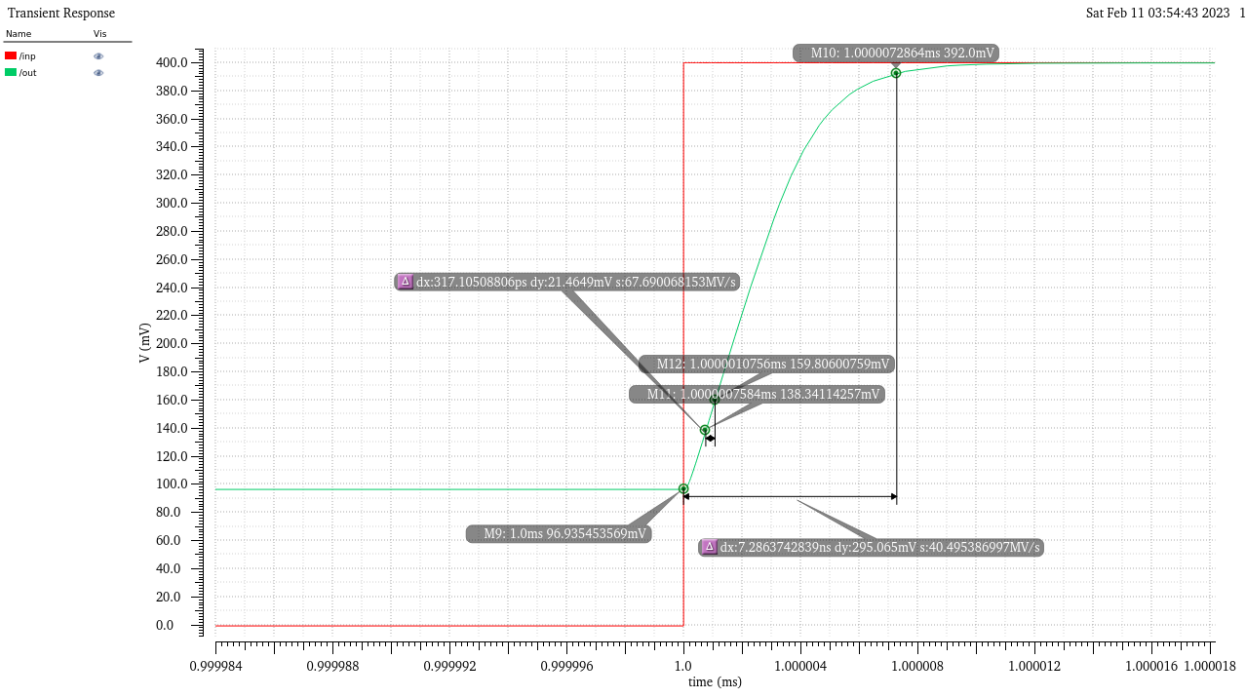

FIGURE 7. CLOSED-LOOP SIMULATION RESULTS FOR SR AND SETTLING TIME.

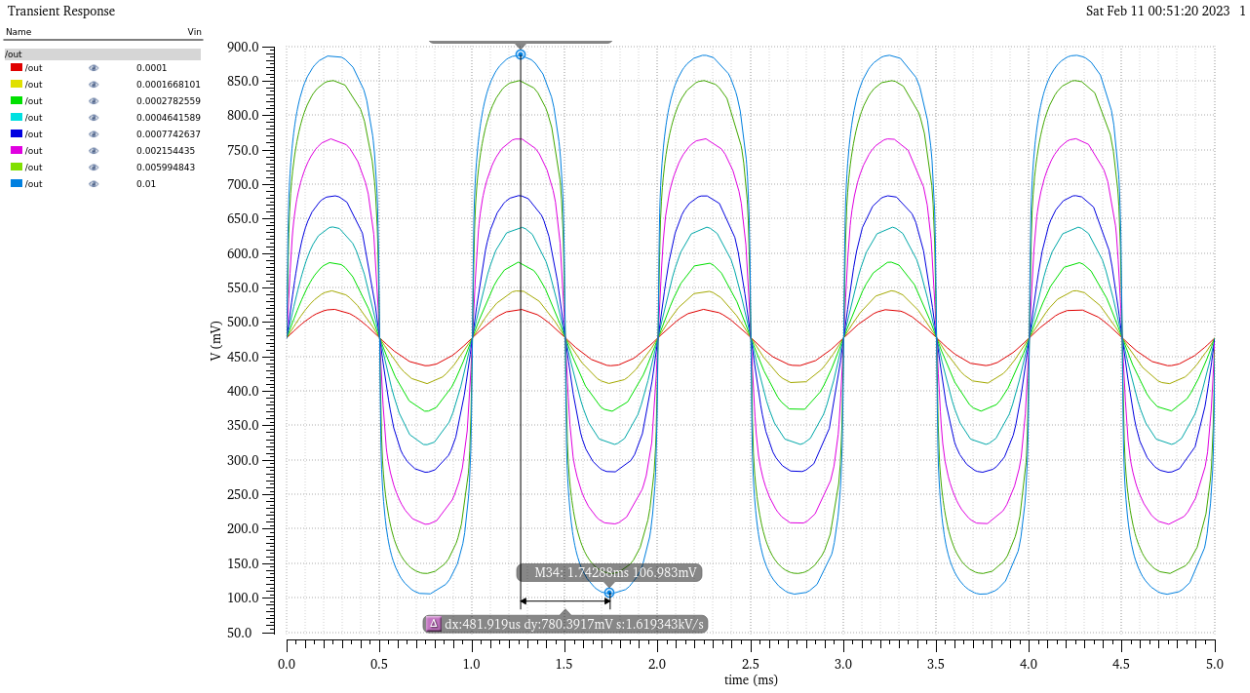

FIGURE 8. OUTPUT SWING VS. SMALL-SIGNAL INPUT.

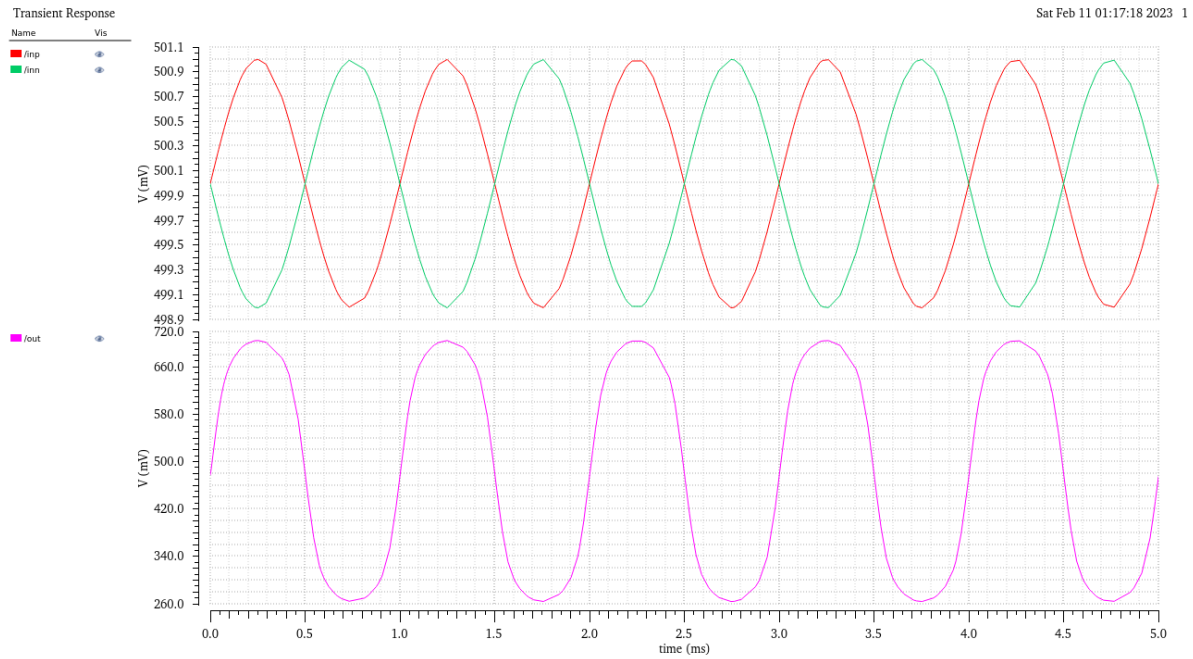

FIGURE 9. TRANSIENT RESPONSE OF THE OTA AT 1 KHZ INPUT.

Metric	Our results
DC gain (dB)	52
UGBW (MHz)	186.9
Slew rate (MV/s)	67.7
2% settling time (ns)	7.3
Phase margin (deg)	101
Total power consumption (uW)	99
Total current consumption (uA)	99
Max output swing (mV)	781

TABLE 2. PERFORMANCE METRICS AND RESULTS.

References

[1] ECEN 474/704 Lab 7: Operational Transconductance Amplifiers. https://people.engr.tamu.edu/spalermo/ecen474/Lab7.pdf

[2] F. Silveira, D. Flandre, and P. G. A. Jespers, “A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA,” *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996.