Design, Analysis and Simulation of a 16 Gbps I/O Link

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***Abstract*—This work demonstrates the design of 16 Gbps high-speed link operating at 16 dB channel loss. The transmitter (TX) consists of 4:1 serializer, clock buffers, predrivers, segmented Voltage Mode (VM) driver with source-series termination (SST) and 3-tap feedforward equalization (FFE). On the receiver side (RX), we implement active Continuous Time Linear Equalizer (CTLE) along with quarter rate slicers. Various performance metrics are provided at the end of the paper. Energy efficency of 0.766 pJ/bit is reported. All the circuits are implemented in TSMC65 PDK.**

***Index Terms*—High-speed links, Voltage-mode driver, TXLE, CTLE, energy-efficiency.**

I. Introduction

HIGH-speed links play an important role in data transmission applications. Therefore, it is essential to push the data rate further while keeping the power consumption low. In this regard, on an architectural level, this work proposes to use 3-tap TX linear equalizer (TXLE) with active CTLE at the RX side.

When it comes to the circuit level decisions, Voltage Mode (VM) driver with 3-tap feed-forward equalization and 50 Ω matching with a tunability range of ±30% can run at 16 Gbps while consuming significantly less power compared to its Current Mode Logic (CML) alternatives [1]. The tradeoff that we pay is, however, the complex segment allocation logic and its issues in layout. Another reasonable concern is the variable R_{ON} of transistors. Based on the preliminary MATLAB simulations, a standalone 3-tap TXLE (1 pre-cursor, 1 cursor, and 1 post-cursor) can provide adequate eye opening (Figure 1). However, these results are optimistic as they are very abstract. Circuit level simulations in Cadence Virtuoso demonstrated that a standalone TXLE is not enough to provide error-free transmission at 16 Gbps due to severe ISI even after the equalization. In this way, it was decided to incorporate CTLE into the transceiver architecture. Particularly, active CTLE is very useful when it comes to boosting the high-frequency components of signals. Additionally, if designed properly, they are able to improve the channel response across all the frequency ranges and make it more flat.

II. TX Architecture Implementation

The VM driver architecture as described before is based on independent control of de-emphasis and impedance. We utilize binary weighted de-emphasis with 3 bits of resolution, which leads to 3 different p-over-n devices with size 1x, 2x, 4x. For impedance matching and subsequent tuning we use 200 Ω resistance for pull-up ($R_{ON,PMOS} + R_u$) and pull-down

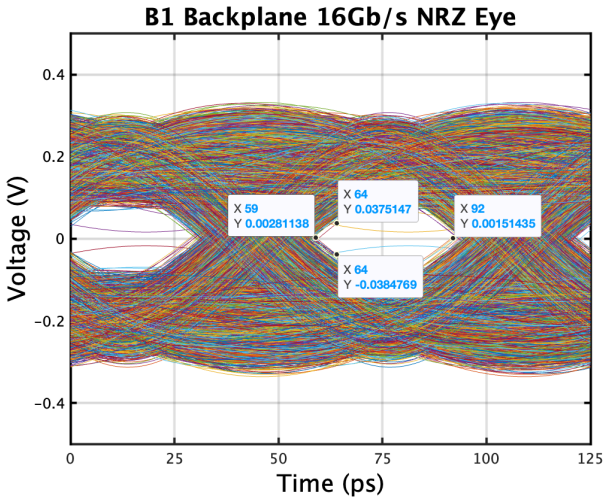

Fig. 1. 3-tap TX FIR equalized eye diagram at 16 Gbps with worst-case bit responses highlighted.

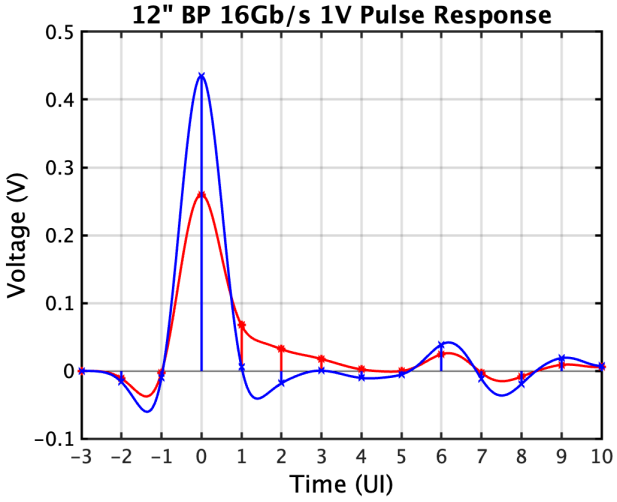

Fig. 2. 3-tap TX FIR equalization pulse response (red) vs. 3-tap TXLE with CTLE pulse response (blue) at 16 Gbps.

($R_{ON,NMOS} + R_d$) and select the values R_d and R_u based on the on-resistance of the MOSFETs (expected to be around 45 Ω). We then combine 6 such identical p-over-n structures where each PU and PD paths have 200 Ω resistance. This allows us to tune the TX output resistance from 36.5 Ω up to 104 Ω with 2.6 bits of resolution. The circuit for the driver is illustrated in Figure 3.

The VM driver is preceded by 4:1 serializer and predrivers. Because everything on TX side is based on CMOS levels,

the predriver is simply a chain of inverters with different sizes. The sizing is performed based on the logical effort analysis and simulation results. The circuit is depicted in Figure 4, where 6 cascaded inverters are shown with FO3.2 sizing each. Thus, while the first stage consists of minimum length & width transistors (C_{inv}), the last stage transistors have 336*C_{inv} sizing. The sizing was performed by first measuring predriver's load capacitance - VM driver. This was accomplished by applying a ramp signal from 0 to VDD and integrating the current at the input of the driver. Based on this method, we estimate the input capacitance of the VM driver to be approximately 187 fF for the case when there is no de-emphasis.

The serializer architecture is based on the well-established references [2]-[3] and thus employs half rate tree-MUX structure with cascaded 2:1 stages. The schematic is presented in Figure 5, where one can notice 5 2:1 MUXes, 7 D flip-flops (DFF), and no D-latches. As usual, the first half-rate MUX (i.e. the one after the 3 DFFs) outputs the pre-cursor, the second outputs the cursor, and the third produces the post-cursor signals. To effectively utilize the half-rate architecture, we also omit D-latches since our devices functions correctly even without them. The basic building block of the serializer is essentially a five-latch 2:1 MUXes. The elements in the first and subsequent stages are being driven by 4 GHz and 8 GHz clocks, respectively. Also, it is worthing mentioning that 2:1 MUXes are built using transmission gate (TG) logic since it provides the fastest speed with very little power consumption (Figure 6). The output of MUXes are restored to CMOS levels in the predriver stages. We use 2 separate clocks for each frequency since we are not required to design any clock dividers. Two opposite phases are required for the serializer, which is implemented using the chain of inverters that are matched to have identical delays (Figure 7). The entire TX architecture is depicted in Figure 8).

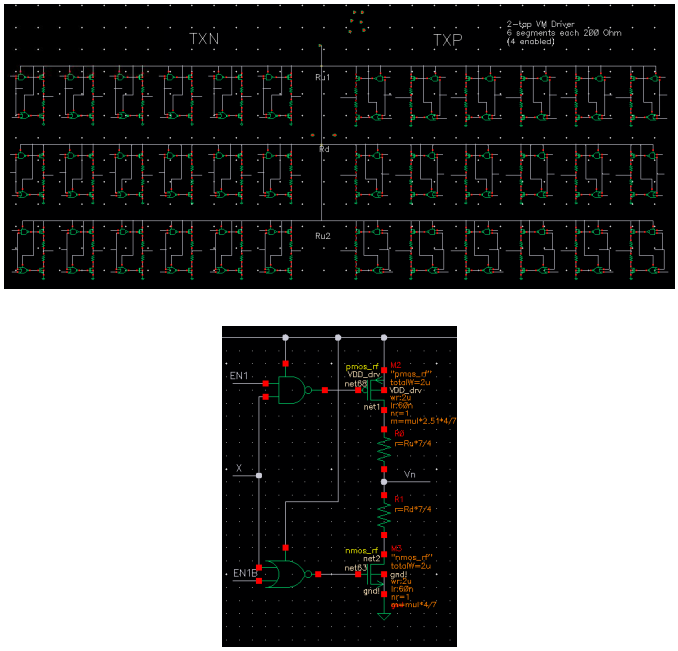

Fig. 3. 2-tap FIR VM driver with segment allocation logic (top) and zoomed in view of a single block (bottom).

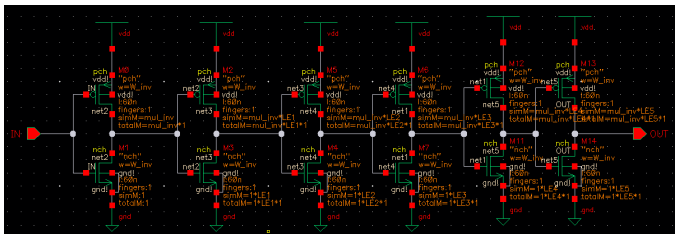

Fig. 4. CMOS predriver.

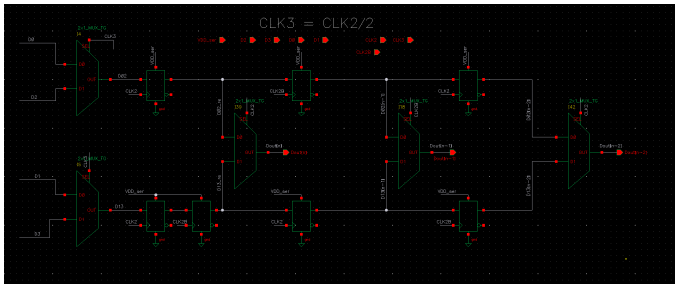

Fig. 5. CMOS serializer.

III. RX Architecture Implementation

As mentioned before, the RX side includes CTLE followed by quarter rate T/H switches and slicers. We also implemented RX clock buffers following the same principles as on TX side.

In order to accurately build and size the devices, one has to start designing the RX side from the reverse, i.e. starting from SAL comparators and finishing with any analog front-end device such as CTLE. This is done so that one can precisely estimate the load capacitance for the preceding stage.

The slicer architecture is based on popular StrongArm latch (SAL) implementation [4] in NMOS configuration since our far-end signal common-mode is above 500 mV. The schematics of the SAL and the subsequent SR latch are shown in Figure 9-10. Because we utilize quarter rate architecture, the timing requirements are alleviated and the transistor sizes are not large, leading to lower power consumption too. For the SR latch we implement 4 transistor based architecture so as to reduce the number of transistors and save power [5]. Next, Figure 11 illustrates the T/H switch realized through TG. Therefore, each T/H switch requires two opposite phases of clock signal. Note that on the RX side, all the clock signals are delayed by the channel delay so as to precisely align the clock to the ideal sampling point.

Running at full-rate and working with small-signals, the CTLE architecture is severely constrained by the factors. However, because of quarter rate architecture and relatively small input capacitance from SAL comparators, the load capacitance is not large, constituting around 10 fF. With this in mind, by defining the target specification following the MATLAB simulations, we design the CTLE to have Rs = 1600 Ω, Cs = 39 fF, and with DC current of 300 uA. This leads to the frequency response as shown in Figure 14.

TABLE I
SPECIFICATIONS TABLE.

	Specifications	Achieved results
VDD used	1V	1V
Data rate	16 Gbps	16 Gbps
Total link power consumption	Minimum	12.25 mW
TX total power consumption	Minimum	11 mW
Clock buffer power consumption	Minimum	201 μW
Serializer power consumption	Minimum	230 μW
Predriver power consumption	Minimum	1.212 mW
Driver power consumption	Minimum	9.56 mW
RX total power consumption	Minimum	1.05 mW
Slicer power consumption	Minimum	144 μW
Synchronizer power consumption	Minimum	84.6 μW
CTLE power consumption	Minimum	825 μW
Energy efficiency of link	Minimum	0.766 pJ/bit
Eye opening at RX	Maximum	30 mV vertical and 26 ps horizontal opening

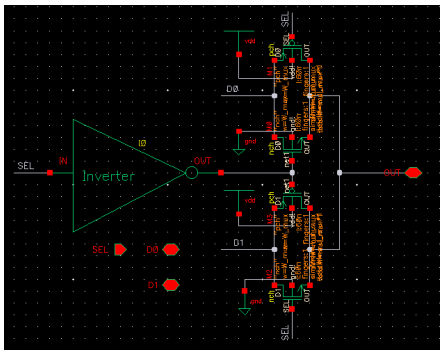

Fig. 6. 2:1 TG MUX.

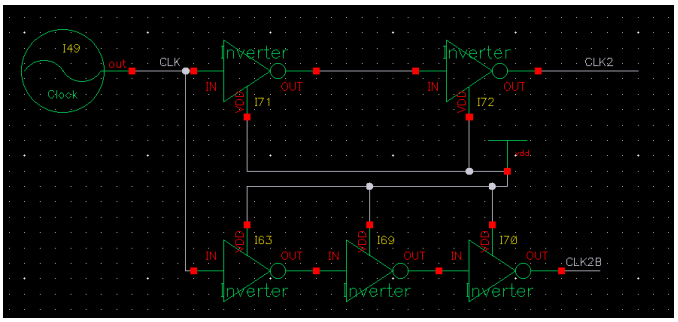

Fig. 7. Clock buffers for TX.

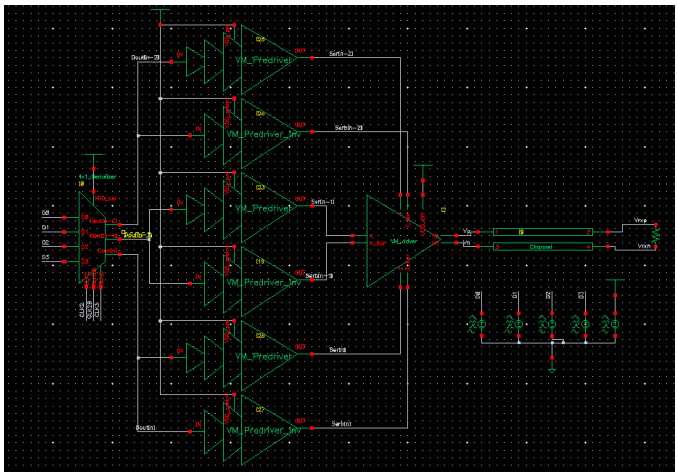

Fig. 8. Overall TX architecture.

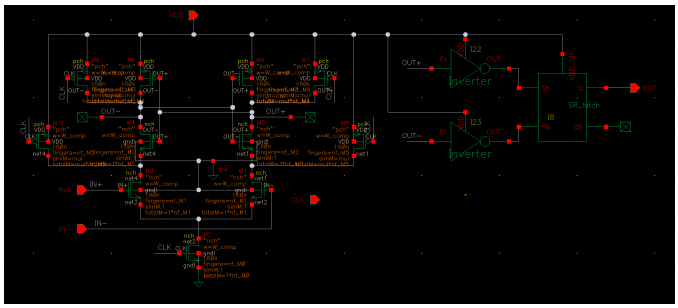

Fig. 9. SAL comparator schematics.

IV. RESULTS

Next, we present the circuit level simulation results. We first conduct worst-case (WC) response analysis in Cadence and compare it to the results obtained in MATLAB to verify that the proposed transceiver is working properly. According to Figures 18-21, circuit level simulations agree very well with MATLAB analysis. It is worth mentioning that to send this WC bit pattern, we first split the actual bit pattern into 4 individual arrays so that they can be serialized properly and the resulting bit sequence matches to the MATLAB code. Note that we introduce 100 UI delay between WC0 and WC1 bit sequence in Cadence so as to eliminate their ISI effects on each other. The WC eye diagram is also provided (Figure 22). In this way, it can be definitely concluded that the proposed transceiver can send error-free data at 16 Gbps even in the worst-case scenario.

We also ran transient simulation to demonstrate the efficacy

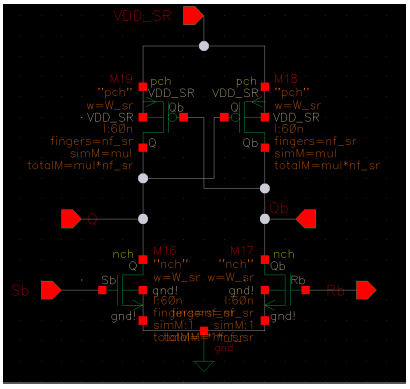

Fig. 10. SR latch schematics.

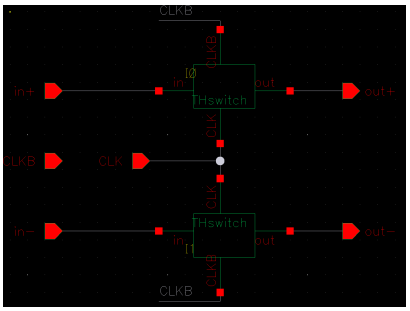

Fig. 11. T/H switch schematics.

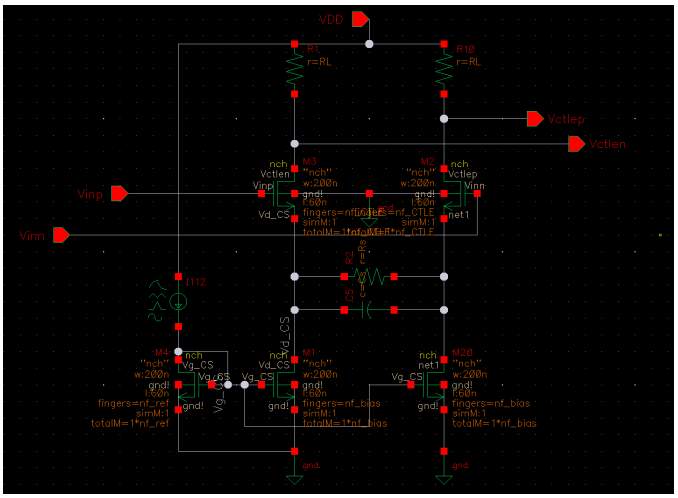

Fig. 12. Active source degeneration CTLE architecture.

of CTLE over standalone TXLE. This is displayed in Figure 23, where one can notice noticeable benefits of having active CTLE. From the same figure one can also see that our VM driver can indeed emphasize the transitions and de-emphasize the DC part of the signal. Figure 24 demonstrates this more vividly, showing all the possible signal levels. We also analyze the TX output impedance in Cadence by running s-parameter analysis. Based on Figure 25, we can adjust the impedance from 36 Ω up to 106 Ω, which is more than the required specification.

The eye diagrams on RX side are provided in Figures 26-27. Furthermore, the PRBS checker response is shown in Figure

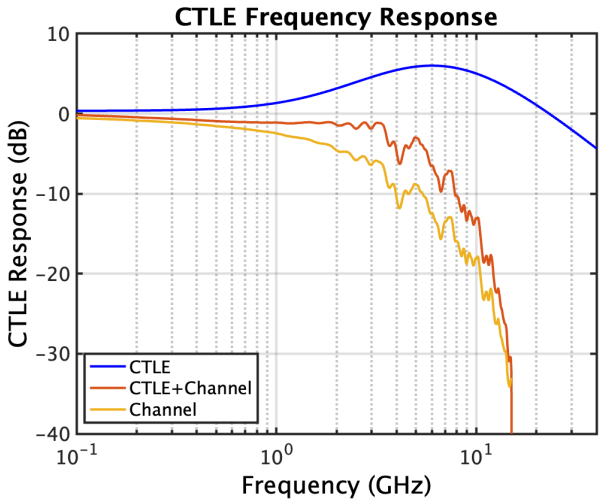

Fig. 13. Benefit of CTLE visualized.

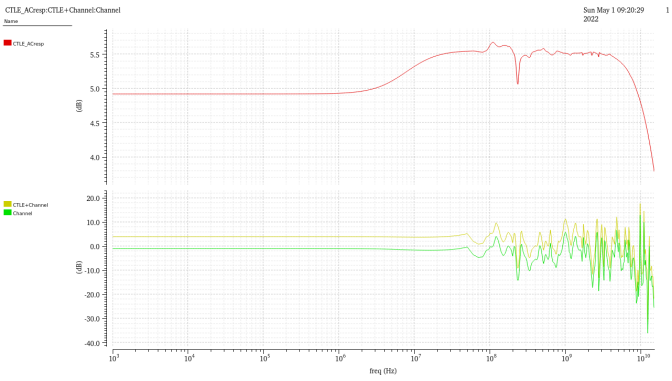

Fig. 14. CTLE frequency response in Cadence. The red waveform is the AC response of CTLE only; the green waveform is the AC response of the channel; the yellow curve is the response from combined CTLE and channel. One can notice up to 5 dB gain at Nyquist frequency.

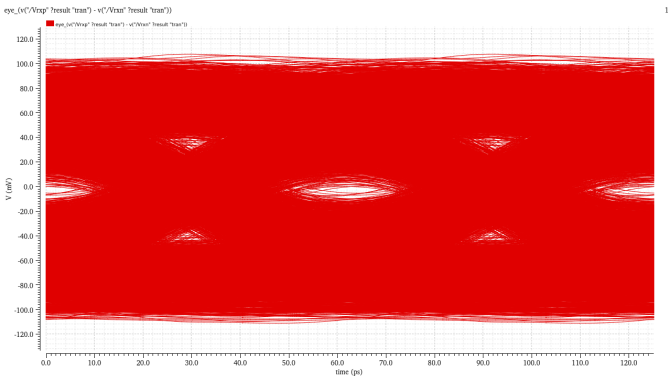

Fig. 15. Eye diagram with TXLE but no CTLE.

28. According to this figure, there are no errors made by our transceiver for the entire 10000 bits.

Finally, we analyze the power consumption of each block at TX and RX as well as the energy-efficiency of the entire link. The results are presented in Table I.

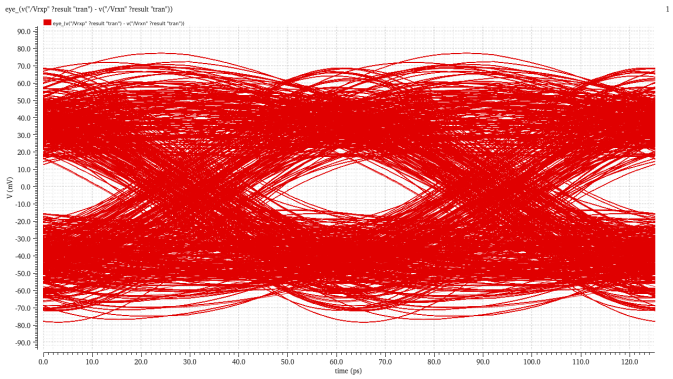

Fig. 16. Eye diagram with TXLE and CTLE.

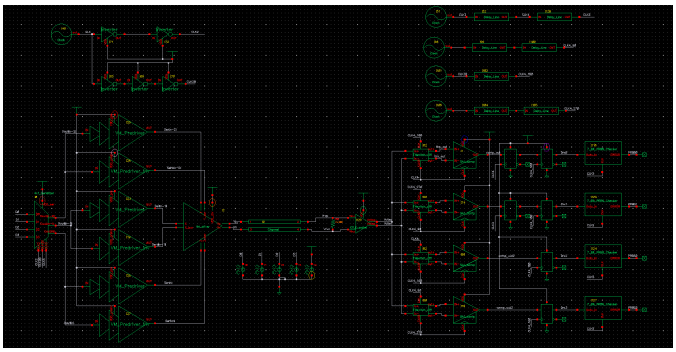

Fig. 17. Complete link schematics.

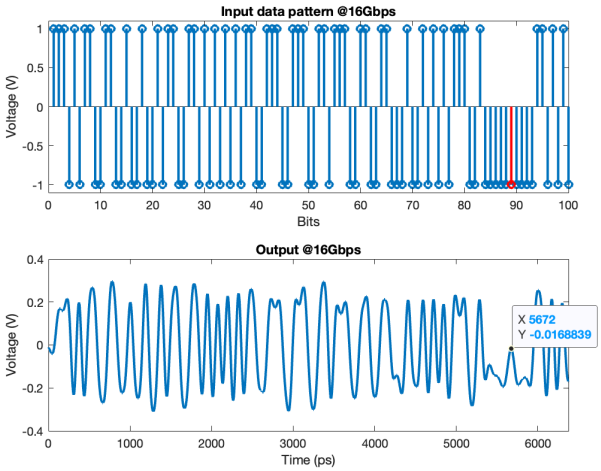

Fig. 18. WC0 response simulated in MATLAB.

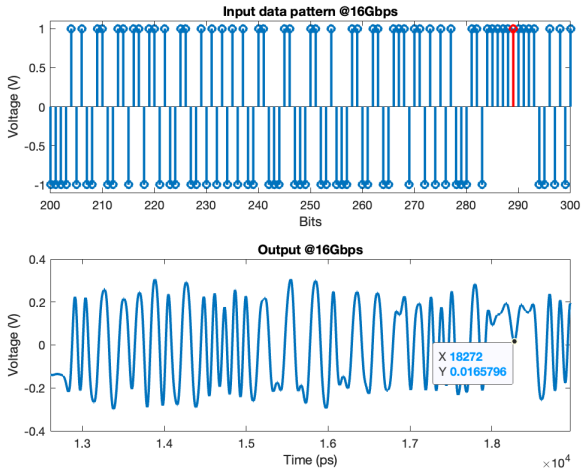

Fig. 19. WC1 response simulated in MATLAB.

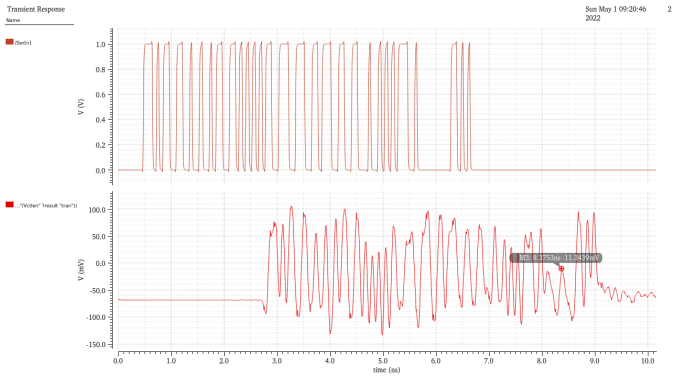

Fig. 20. WC1 response simulated in Cadence.

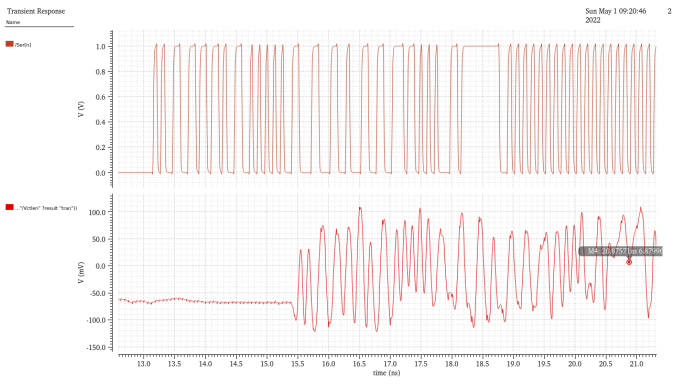

Fig. 21. WC1 response simulated in Cadence.

V. Conclusion

In summary, this report provided circuit level description of the 16 Gbps transeiver link architecture. The error free operation for 10000 UI was verified and various analysis was conducted to ensure proper working of the proposed link. Several key architectural decisions allowed us to achieve 0.766 pJ/bit of energy-efficiency.

VI. References

[1] Y. Song, H. Yang, H. Li, P. Y. Chiang and S. Palermo, ”An 8–16 Gb/s, 0.65–1.05 pJ/b, Voltage-Mode Transmitter With Analog Impedance Modulation Equalization and Sub-3 ns Power-State Transitioning,” in IEEE Journal of Solid-State Circuits, vol. 49, no. 11, pp. 2631-2643, Nov. 2014, doi: 10.1109/JSSC.2014.2353795.

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[3] J. F. Bulzacchelli et al., ”A 10-Gb/s 5-Tap DFE/4-Tap FFE

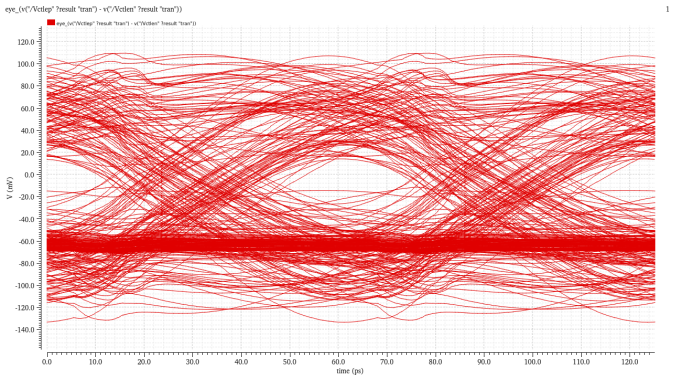

Fig. 22. WC eye diagram after CTLE.

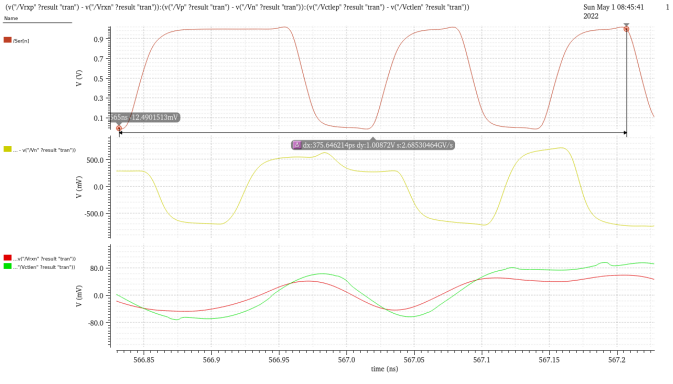

Fig. 23. 6 UI transient waveform of the serialized input of the VM driver (red), it's output before the channel (yellow), received signal before CTLE (red), and received signal after CTLE (green).

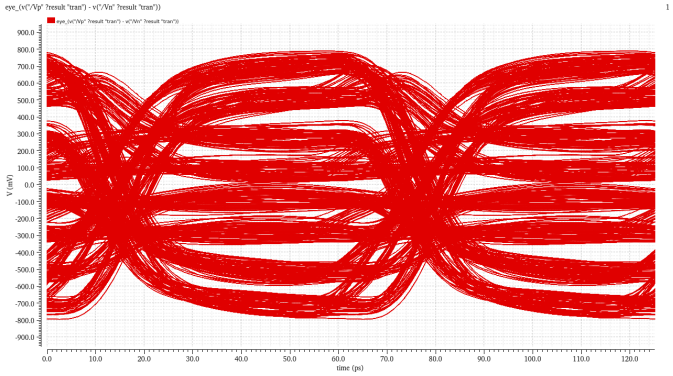

Fig. 24. 10000 bits eye diagram at the output of TXLE (before channel).

Transceiver in 90-nm CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 41, no. 12, pp. 2885-2900, Dec. 2006, doi: 10.1109/JSSC.2006.884342.
[4] M. Matsui et al., "A 200 MHz 13 mm/sup 2/ 2-D DCT macrocell using sense-amplifying pipeline flip-flop scheme," in IEEE Journal of Solid-State Circuits, vol. 29, no. 12, pp. 1482-1490, Dec. 1994, doi: 10.1109/4.340421.
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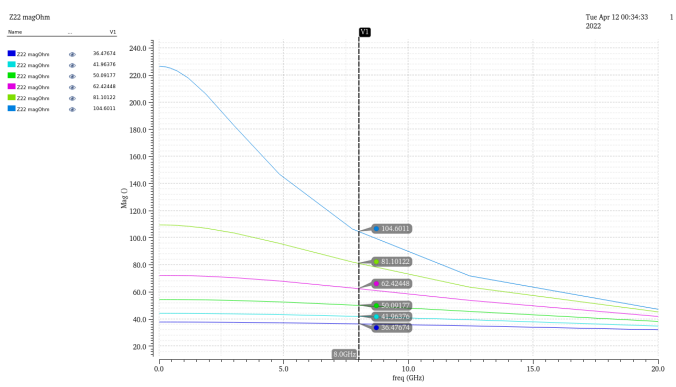

Fig. 25. TXLE output impedance.

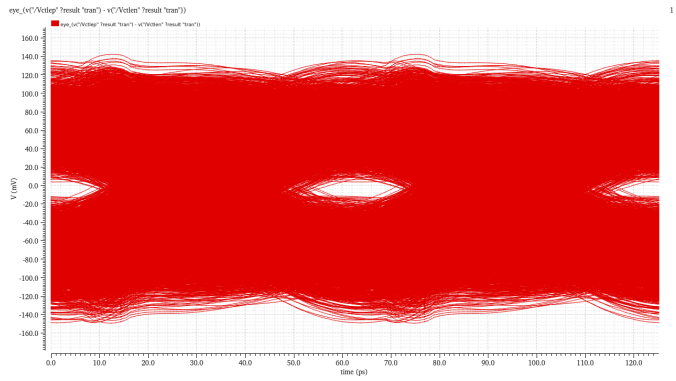

Fig. 26. 10000 bits RX eye diagram after CTLE.

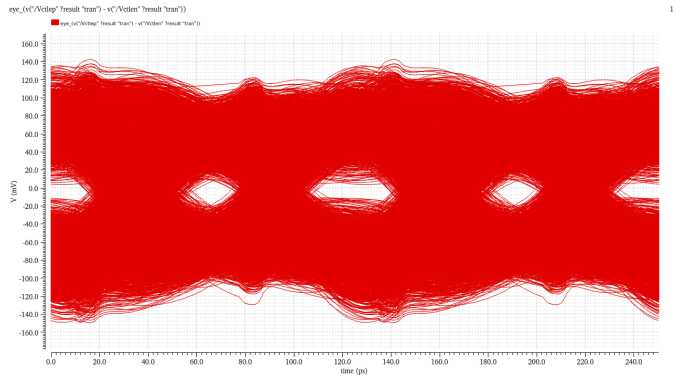

Fig. 27. 10000 bits RX eye diagram after CTLE for quarter rate clocking.

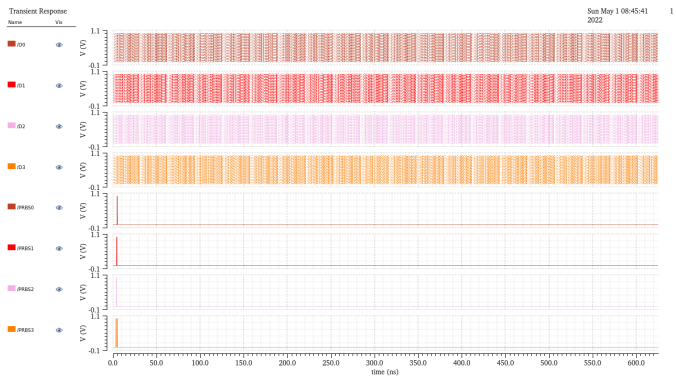

Fig. 28. PRBS checker output for 10000 bits.

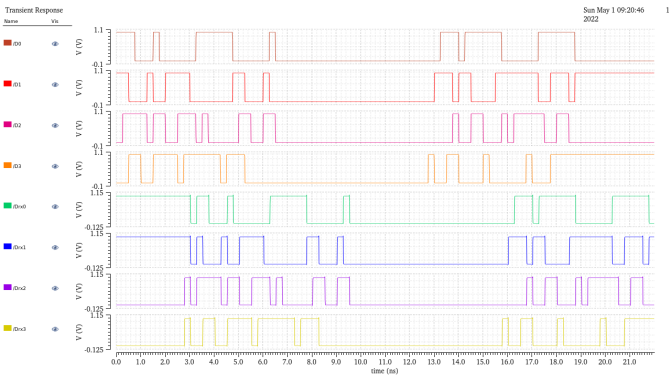

Fig. 29. WC sequence (100 bits of WC0 + 100 UI + 100 bits of WC1) correctly recovered at RX output (observed after the synchronizer and before the PRBS checker).