Dias Azhigulov

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Education

University of British Columbia **Vancouver, BC**
M.A.Sc. in Electrical and Computer Engineering, 89.8/100 GPA Jan 2021–Nov 2023 (expected)
Coursework: Analog IC design, PLLs, High-speed links, Digital VLSI systems, Silicon Photonics, Machine Learning

Nazarbayev University **Astana, Kazakhstan**
B.Eng. with Honors in Electrical and Electronic Engineering, 3.73/4.00 GPA Aug 2016–Jun 2020
Coursework: Programming, Microcontrollers, Computer architecture, PCB design, Digital & Analog IC design and layout, Power electronics, Deep Learning, Signal processing, Numerical optimization, HDL modelling of electronics.

Skills

Technical skills: Cadence Virtuoso, Schematic & layout design, Corner & MC simulations, g_m/I_d design, Cadence Genus, Calibre DRC, LVS, PEX, Quartus Prime, ModelSim, KLayout, Verilog-A, Verilog, Lumerical Suite, MATLAB, Python, Linux, Shell scripting, SKILL.

Experience

System-on-Chip Lab, University of British Columbia **Vancouver, BC**
Graduate Research Assistant Feb 2021–Present
- Taped out the 1.2V Bandgap Voltage Reference circuit in TSMC65. The maximum PVT variation was reduced down to 28 mV across all PVT corners. Also developed and post-layout verified the 1V and 2.5V versions of the circuit for the next run.
- Developed the library of Verilog-A models of Silicon Photonics (SiP) devices. It includes such features as: noise & Monte-Carlo simulations; bidirectional & WDM signalling through single wire; SKILL scripted ports; S-parameter based models using Python script; fast and accurate simulation of chromatic and polarization mode dispersion as well as higher-order optical non-linearities; laser phase noise.
- Collaborated with fellow labmates in building a new PDK for the "SiEPICfab Shuksan" laser integration workshop using in-house developed layermap and technology files. The PDK features schematic-driven layout design for SiP devices, runs natively in Cadence Virtuoso, and supports electro-optic co-simulation. Also wrote SKILL scripts to create CDF netlisting and to generate PCells for layout.
- Designed NAND logic devices based on Mach-Zehnder Modulators and Ge photodetectors for scalable optical switch networks. The electro-optic simulation was performed in Cadence Virtuoso (through custom Verilog-A behavioral models). The chip was sent for fabrication to AMF Singapore.
- Ran measurement tests on two SiP chips fabricated by AMF Singapore and Applied Nanotools Inc. Tested devices include slotted waveguides, ring resonators, mode converters, and MZIs.
- Designed Fabry-Perot cavities for laser applications along with MZI and Michelson interferometers. Performed experimental parameter extraction (coupling coefficient, Q-factor, effective index) from the chip measurements and compared the results with simulation.

Introduction to Microcomputers, University of British Columbia **Vancouver, BC**
Graduate Teaching Assistant Aug 2022–Dec 2022 (Seasonal, 2021 & 2022)
- Collaborated with 3 TAs and instructor to deliver workshops on Linux and Git to undergraduate students.
- Led lab sessions and tutorials involving DE1-SoC FPGA board programming for 20+ students.

Marvell Semiconductor Inc. Canada **Vancouver, BC (remote)**
Optics Engineer Intern May 2022 – Aug 2022
- Enabled electro-optic cosimulation of coherent link in Cadence Virtuoso by creating a Verilog-A SiP library. Using the library designed and simulated 100 Gbps DP-QPSK coherent link that includes active and passive photonics elements and transistor-level drivers and TIAs (45 nm CMOS).
- Helped in integration and debugging of Synopsys Optocompiler for electro-optic cosimulation.

"Fund for supporting research and development of artificial intelligence" CF **Astana, Kazakhstan**
Data Scientist Sep 2020–Feb 2021

- Wrote a program in Python that extracts various statistical data about phone call recordings (SNR, speech length etc.) and preprocesses them along with open-source datasets for Automatic Speech Recognition. Used this preprocessed dataset, which is comprised of bilingual speech, to train hybrid neural network models in Kaldi and achieved 43% WER within 3 months of model development.
- Built robust scalable address converter in Java via Apache Lucene and Regex. The final accuracy is 91% (i.e. the program can match 91 out of every 100 raw addresses), the time it takes to find matches from database to 10000 inputs is 1 hour. The matched addresses are used to obtain their approximate geocoordinates via ArcGIS engine.

Data Analytics Lab, Nazarbayev University **Nur-Sultan, Kazakhstan**
Undergraduate Research Assistant Oct 2019–May 2020

- Developed a Machine Learning based web-application which can in live mode detect different cancers and determine the type of cancers with an accuracy of over 99% based on the images uploaded by a user. Frontend is implemented in Python Flask, Backend is built via Keras and consists of 9 CNNs.
- Organized a team to build a pipeline for preprocessing and classifying human brain signals with Transfer Learning.

iDSN Lab, Nazarbayev University **Astana, Kazakhstan**
Undergraduate Research Assistant Sep 2018–May 2020

- Designed seven basic SiP logic gates in Ansys Lumerical through microring resonators and Ohmic heaters. Results are published in several SPIE conferences and in an academic journal.

Integrated Circuits & Systems Lab, KAUST **Thuwal, Saudi Arabia**
Visiting Student May 2019–Aug 2019

- Designed several CMOS-compatible NEM relay-based power converters (DC/DC, AC/DC, and DC/AC) using switched-capacitor topology in Cadence. Results are published in the ISCAS 2020 conference proceeding.

Projects

- Designed two-stage OTA in 45 nm CMOS using g_m/I_d sizing for target specs. Achieved 52 dB gain, 187 MHz UGBW, 7 ns settling time, 800 mV output swing while consuming 99 μW power.
- Designed analog sub-sampling (SS) LC-PLL in 65 nm CMOS operating at 2.3-2.5 GHz with 100 MHz step size. SS PD and LF are made of switched-capacitor resistor and external capacitor. FLL was synthesized using Verilog and Cadence Genus. Achieved ref. spurs of -71 dB and 670 ns settling time with power consumption of 153 μW (excluding VCO).
- Designed 16 Gbps high-speed I/O link in 65 nm CMOS with mesochronous clocking. TX consists of 4:1 serializer, multi-phase clock generator, predrivers, segmented VM driver with SST and 3-tap FFE. RX is composed of active CTLE, quarter rate slicers (Strong-Arm Latch topology), 4:1 synchronizer. Energy efficiency of 0.766 pJ/bit was achieved.
- Designed 25 Gbps SiP data transmission link in Cadence Virtuoso (65 nm CMOS). The link consists of CW laser, CMOS driver, MRM, PD, and TIA. SiP devices are modelled in Verilog-A. The driver has cascode common-source topology whereas the TIA is based on 3-stage inverters. Energy efficiency of 1.98 pJ/bit was achieved.
- Had experience designing: 1) variable frequency divider for PLLs with a logic circuit to switch between different frequency bands; 2) variable resistance (0.03-2 GHz freq. range) and varactor based (1.9-3.8 GHz freq. range) Voltage Controlled Oscillators (VCO) for PLLs; 3) clock signal distribution systems (56 ps skew, 375 ps latency, 65 mW power consumption); 4) 6T SRAM cells in Cadence Virtuoso (45 nm CMOS).
- Designed error amplifiers (simple differential pair and cascode configuration) for LDO using LTSpice.
- Optimization of the Wireless Sensor Network: created an algorithm in Python for equal distribution of sensors among base stations by formulating the task as quadratic optimization problem under the constraints of a limited amount of power, communication range, and hardware capability.

Publications

- BCI 2021 (South Korea): "Deep Transfer Learning for Subject-Independent ERP-based BCIs"
- ISCAS 2020 (Seville): "BEOL NEM Relay-Based Inductorless DC-DC Converters"
- Journal of Optical and Quantum Electronics: "High-speed thermally tuned electro-optical logic gates based on micro-ring resonators"
- SPIE Photonics West 2019 (San Francisco): "The design of universal logic gates using micro-ring resonator structures"
- CoCoNet 2018 (Astana): "Analyzing the BitTorrent Ecosystem of Central Asia"